ASTRIAL
SYSTEM ELECTRONICS for AI Innovation

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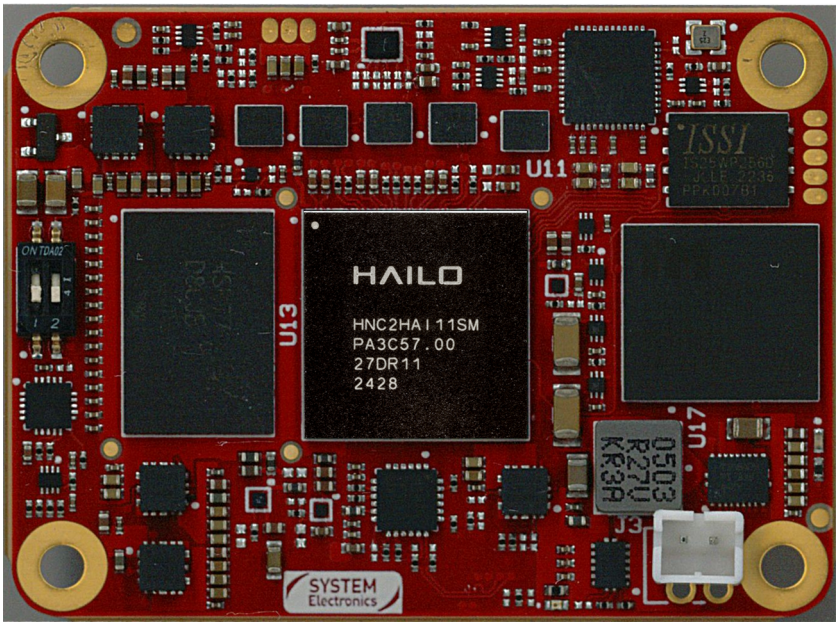
Astrial H15

Technical Manual

System Electronics for AI Innovation



Original instructions

Read this manual before using the equipment

Retain this manual for future use

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Purpose of document

The purpose of this guide is to provide instructions and information for the safe installation and use of the Astrial H15.

Contents

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1 Safety information

This section provides an overview of all safety aspects for the protection of people as well as safe and uninterrupted operation. Other task related safety instructions are included in the specific sections.

1.1 Regulatory compliance

This product meets the safety requirements of the following standards:

EMC directives:

- Directive 2014/30/EU of the European Parliament and of the Council of 26 February 2014 on the harmonisation of the laws of the Member States relating to electromagnetic compatibility.

Environmental directives:

- Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and all addendums current to the date of issue of this declaration.

EMC standards:

- EN IEC 61326-1:2021: Electrical equipment for measurement, control and laboratory use - EMC requirements - General requirements.
- EN IEC 61000-6-2:2019: Electromagnetic compatibility (EMC) - Generic standards. Immunity standard for industrial environments.
- EN IEC 61000-6-4:2019: Electromagnetic compatibility (EMC) - Generic standards. Emission standard for industrial environments.

Emission standard for industrial environments:

- EN IEC 63000:2018: Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances.

1.2 Safety notices

The following safety notice formats are used in this guide. Safety notices are used at the start of sections or embedded in operating instructions.

Make sure you fully understand and comply with the notices in this guide.

DANGER

Indicates a hazardous situation which, if not avoided, will almost certainly result in death or serious injury.

WARNING

Provides important information to prevent serious problems, for example, the loss of data.

Caution

Provides important information on how to prevent moderate problems.

Information

Provides additional information.

Tip

Provides useful hints and tips.

1.3 Safety regulations

WARNING

Failure to comply may result in serious personal injury and/or damage to property! Follow the safety instructions and all the specifications in this manual.

Only use the Astrial H15 in compliance with the information in the manual and the safety measures.

This is a prerequisite for safe and trouble-free operation.

1.4 Exclusion of liability

System Electronics products are supplied in particular hardware and software configurations adapted to the type of application required.

Any modifications to the configurations of the hardware or software other than those described in the manual exempt System Electronics from liability.

Any use of the Astrial H15 other than that described in the manual exempts System Electronics from liability.

1.5 Non-compliant and non-permitted uses

WARNING

Do not use the Astrial H15 in explosive atmospheres.

WARNING

Do not use the Astrial H15 for any purpose which violates local laws or regulations.

WARNING

- Do not use the Astrial H15 if it has not been installed or maintained according to instructions provided by System Electronics.
- Do not use the Astrial H15 if it has been modified in any way other than according to instructions provided by System Electronics.
- Do not use the Astrial H15 if it is malfunctioning.
- Do not allow untrained personnel to use the Astrial H15.

Information

This information has been prepared with care. However, the instructions described are constantly being revised as needed.

We reserve the right to revise and change the procedures and documentation at any time and without notice.

No claims can be made for changes to the information, illustrations and descriptions in this manual.

1.6 Warnings and precautions

Caution

Electrical shock hazard!

Do not touch the Astrial H15 when it is connected to electrical power.

Caution

Only System Electronics personnel are authorised to carry out repairs or unscheduled maintenance.

Do not attempt to repair the Astrial H15. If the Astrial H15 is malfunctioning, contact System Electronics.

1.7 Damage to the product caused by magnetic fields or electrostatic discharges

Electric fields or electrostatic discharges create an electrostatic hazard which can damage individual components, integrated circuits, equipment or devices and consequently cause malfunctions.

Caution

Risk of damage!

For transport and shipping, use packaging materials that can protect the Astrial H15, for example conductive foam or aluminium foil.

For storage, keep the Astrial H15 in its original packaging.

Before touching the Astrial H15, do one of the following:

- wear an ESD (electrostatic discharge) wristband;
- wear ESD shoes or ESD straps for earthing in ESD areas with conductive floors;
- place the components or equipment on conductive surfaces.

2 Overview of the Astrial H15

2.1 Introduction

The Astrial H15 is an AI-powered System on Module (SoM) designed for edge computing applications, combining high-performance AI vision capabilities with industrial reliability. Built around the Hailo-15 Vision Processor, it delivers top-tier inference performance while maintaining low power consumption – ideal for vision-based embedded systems.

With up to 20 TOPS of AI power, the Astrial H15 enables real-time AI applications like object detection, classification, and segmentation directly on the edge, eliminating the need for cloud processing and enhancing privacy, security, and system responsiveness. The module integrates an ISP (Image Signal Processor) with AI acceleration in a compact design, providing a seamless vision pipeline from image acquisition to inference.

The Astrial H15 offers Gigabit Ethernet, MIPI CSI & DSI, USB 3.0, and PCIe Gen3 interfaces, along with built-in security features such as Secure Boot and hardware cryptography. Its industrial oriented design ensures reliability in harsh environments, making it suitable for applications in industrial automation, smart cameras, autonomous systems, and smart retail.

Key highlights:

- On-the-Edge AI Vision: Real-time, low-latency inference with up to 20 TOPS for computer vision tasks.
- Integrated Vision Pipeline: ISP and AI accelerator on a single chip, simplifying system architecture.
- Dedicated AI Smart Camera features: Noise Reduction, HDR, A-Focus, AWB, A-Exp. Distortion Correction, Motion Compensation & Image Stabilization, Digital zoom, Low Light vision
- Low power consumption, and long-term availability.

The Astrial H15 empowers developers to accelerate AI innovation at the edge, delivering a scalable, ready-to-use platform for the next generation of embedded vision applications.

2.2 Main features

- Hailo H15: 4x A53 + 2x M4 + 20 TOPS
- eMMC: 16G RAM: 4G
- 2x MIPI-CSI 4k 30FPS

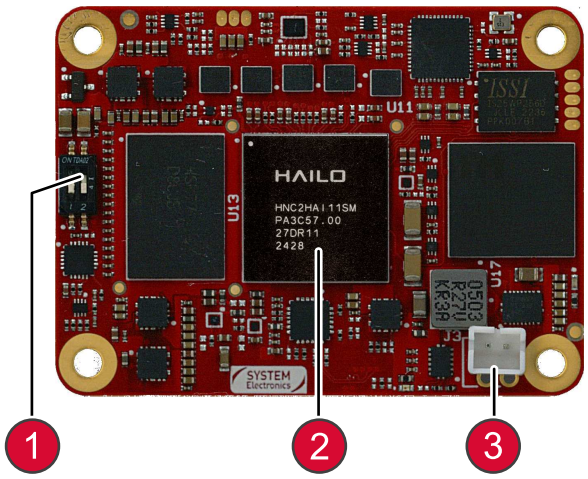
- Dedicated AI Smart Camera features:
  - Noise reduction, HDR, A-Focus, A-WB, A-Exp
  - Distortion correction
  - Motion Compensation & Image Stabilization
  - Digital zoom, Low Light vision

2.3 Highlights

- Compatible CM5 header
- Hailo H15: 4x A53 + 2x M4 + 20 TOPS
- RAM 4 Gbyte LPDDR4 32 bit, eMMC 16 Gbyte
- 2 x MIPI-CSI 4-lanes 4k 30FPS
- 1 x MIPI-DSI 4- lanes
- 1 x PCIe Gen3 4-lanes
- 1 x Gigabit Ethernet PHY
- 1 × USB 2.0, 1x I2S, 2 × UART
- 1x SDIO, 2x I2C
- Dual-ISP for camera interface
- Enhanced IoT EdgeLock® SE050
- Low power design 4W
- 32MB QSPI Flash
- Linux YOCTO Kirkstone/LTS and GitHub support by Hailo
- 32 × GPIO header with alt function

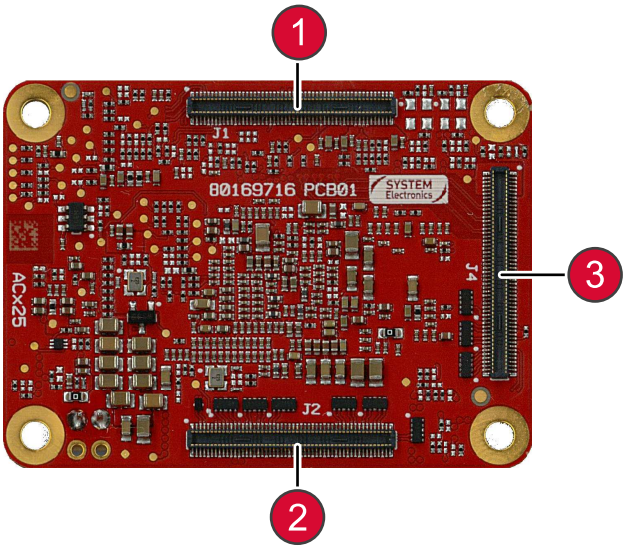
2.4 Astrial H15 components

Figure 1 - Astrial H15 components (front)



1	Boot switch
2	Hailo-15 (H15) processor
3	Auxiliary power connection

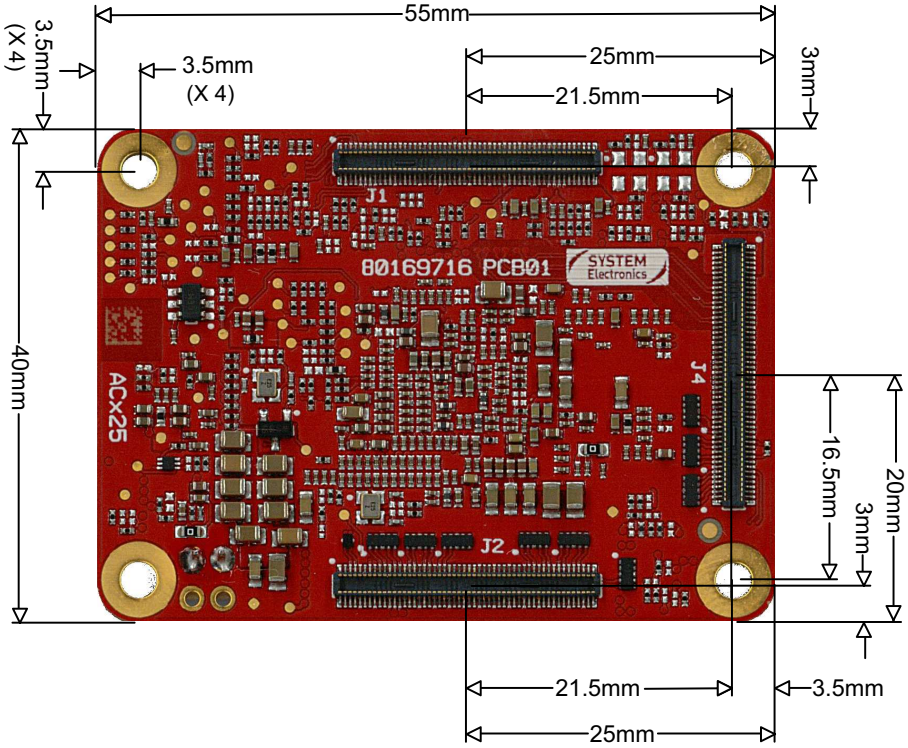
Figure 2 - Astrial H15 components (back)



1	Standard CM5 connector (J1)
2	Standard CM5 connector (J2)
3	Additional third CM5 connector (J4)

2.5 Dimensions

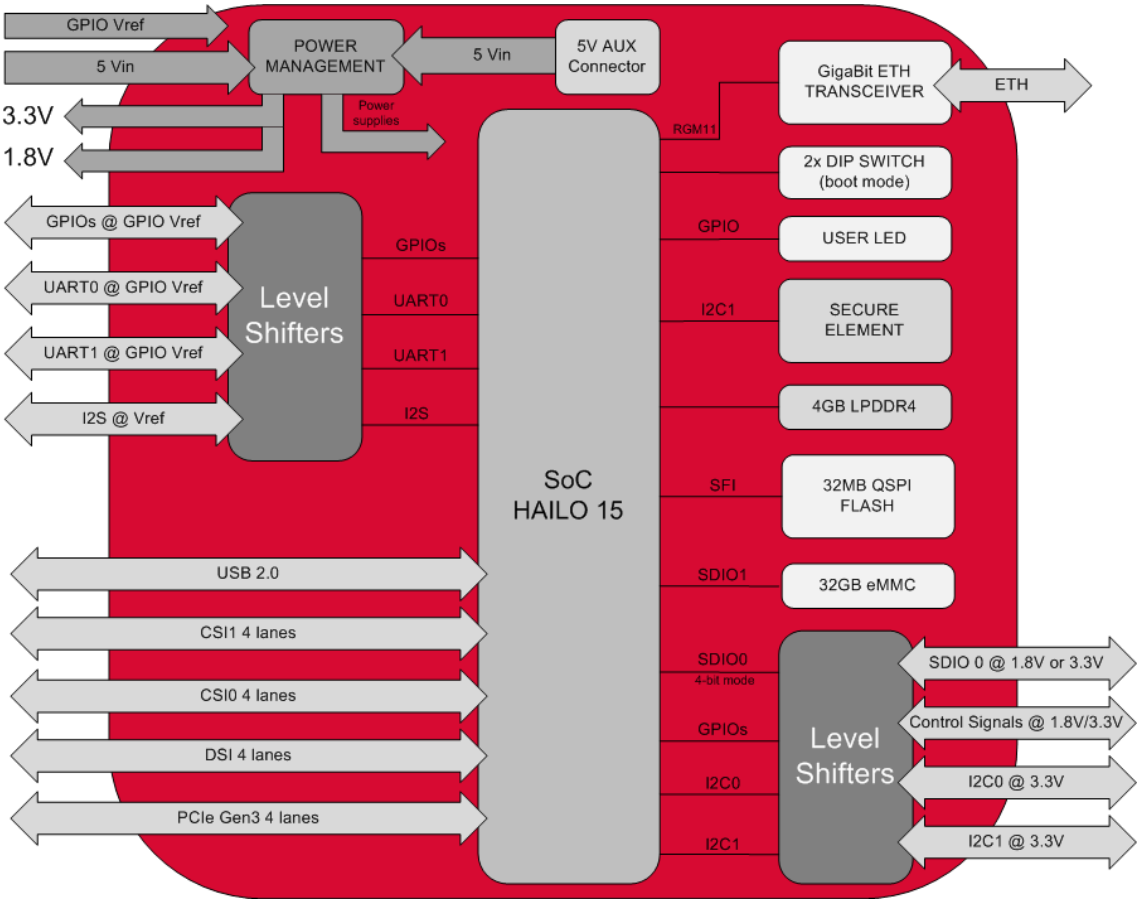
Figure 3 - Astrial H15 dimensions



3 Schematics

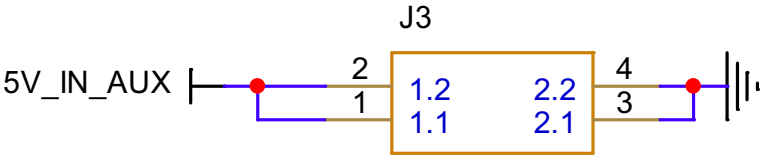
3.1 Block diagram

Figure 4 - Block diagram



3.2 Auxiliary 5 V power connector

Figure 5 - Auxiliary 5 V power connector



Conn. PTSM 0,5/ 2-2,5-V THR WH R44 (1814566)

3.3 Compute module (CM) connectors

Notice

All connectors are compliant with the CM5 standard.

3.3.1 Carrier board connector (J1)

Figure 6 - Carrier board connector (J1)

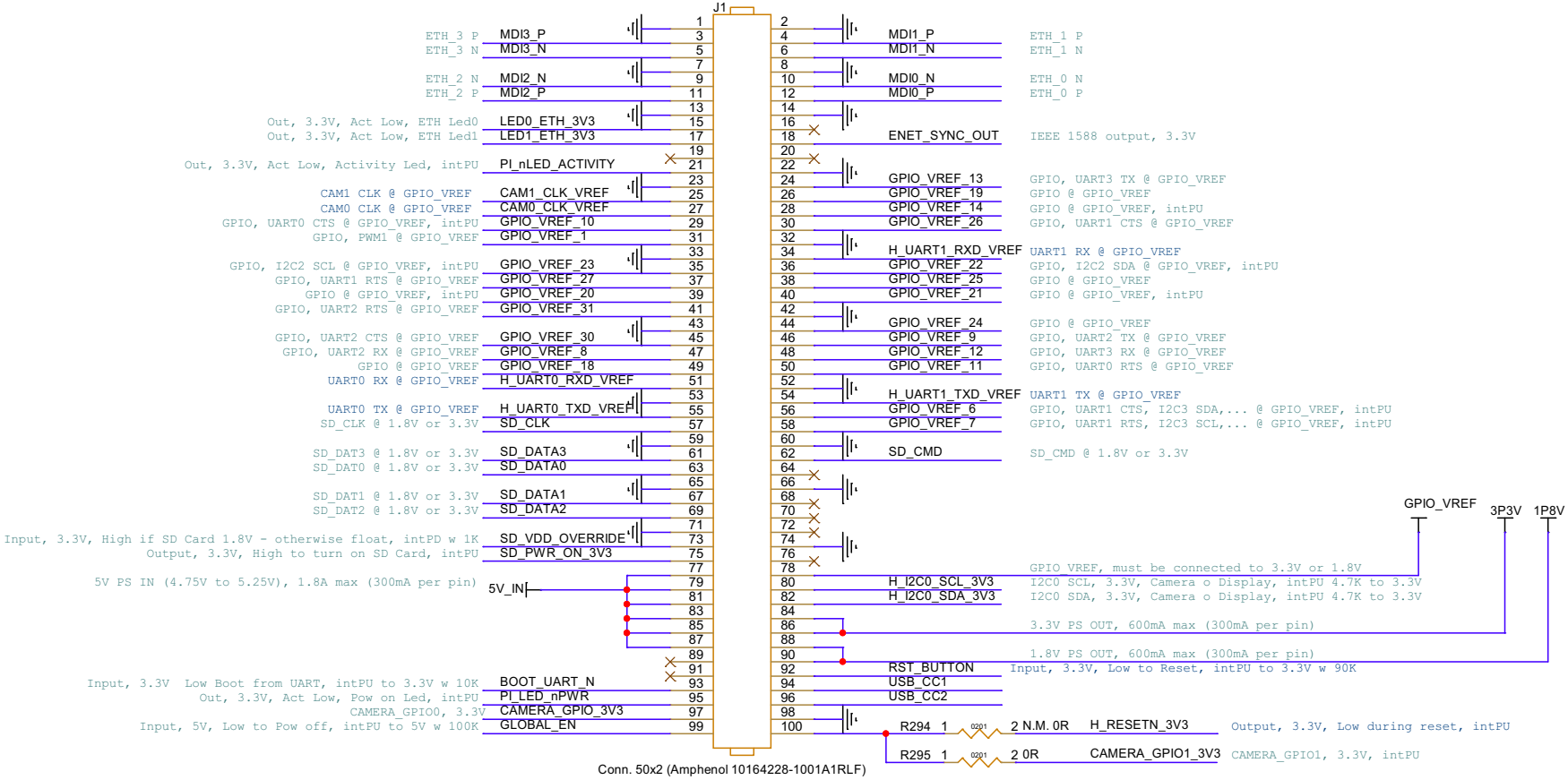


Table 1 - Carrier board connector 1 (J1) pinout

Pin number	Pin name	Pin description
1	GND	GND
2	GND	GND
3	MDI3_P	ETH_3 P
4	MDI1_P	ETH_1 P
5	MDI3_N	ETH_3 N
6	MDI1_N	ETH_1 N
7	GND	GND
8	GND	GND
9	MDI2_N	ETH_2 N
10	MDI0_N	ETH_0 N
11	MDI2_P	ETH_2 P
12	MDI0_P	ETH_0 P
13	GND	GND
14	GND	GND
15	LED0_ETH_3V3	Out, 3.3V, Active Low, ETH LED0
16	NC	
17	LED1_ETH_3V3	Out, 3.3V, Active Low, ETH LED1
18	ENET_SYNC_OUT	IEEE 1588 output, 3.3V
19	NC	

Pin number	Pin name	Pin description
20	NC	
21	PI_nLED_ACTIVITY	Out, 3.3V, Active Low, Activity LED, intPU
22	GND	GND
23	GND	GND
24	GPIO_VREF_13	GPIO, UART3 TX @ GPIO_VREF
25	CAM1_CLK_VREF	CAM1 CLK @ GPIO_VREF
26	GPIO_VREF_19	GPIO @ GPIO_VREF
27	CAM0_CLK_VREF	CAM0 CLK @ GPIO_VREF
28	GPIO_VREF_14	GPIO @ GPIO_VREF, intPU
29	GPIO_VREF_10	GPIO, UART0 CTS @ GPIO_VREF, intPU
30	GPIO_VREF_26	GPIO, UART1 CTS @ GPIO_VREF
31	GPIO_VREF_1	GPIO, PWM1 @ GPIO_VREF
32	GND	GND
33	GND	GND
34	H_UART1_RXD_VREF	UART1 RX @ GPIO_VREF
35	GPIO_VREF_23	GPIO, I2C2 SCL @ GPIO_VREF, intPU
36	GPIO_VREF_22	GPIO, I2C2 SDA @ GPIO_VREF, intPU
37	GPIO_VREF_27	GPIO, UART1 RTS @ GPIO_VREF
38	GPIO_VREF_25	GPIO @ GPIO_VREF
39	GPIO_VREF_20	GPIO @ GPIO_VREF, intPU

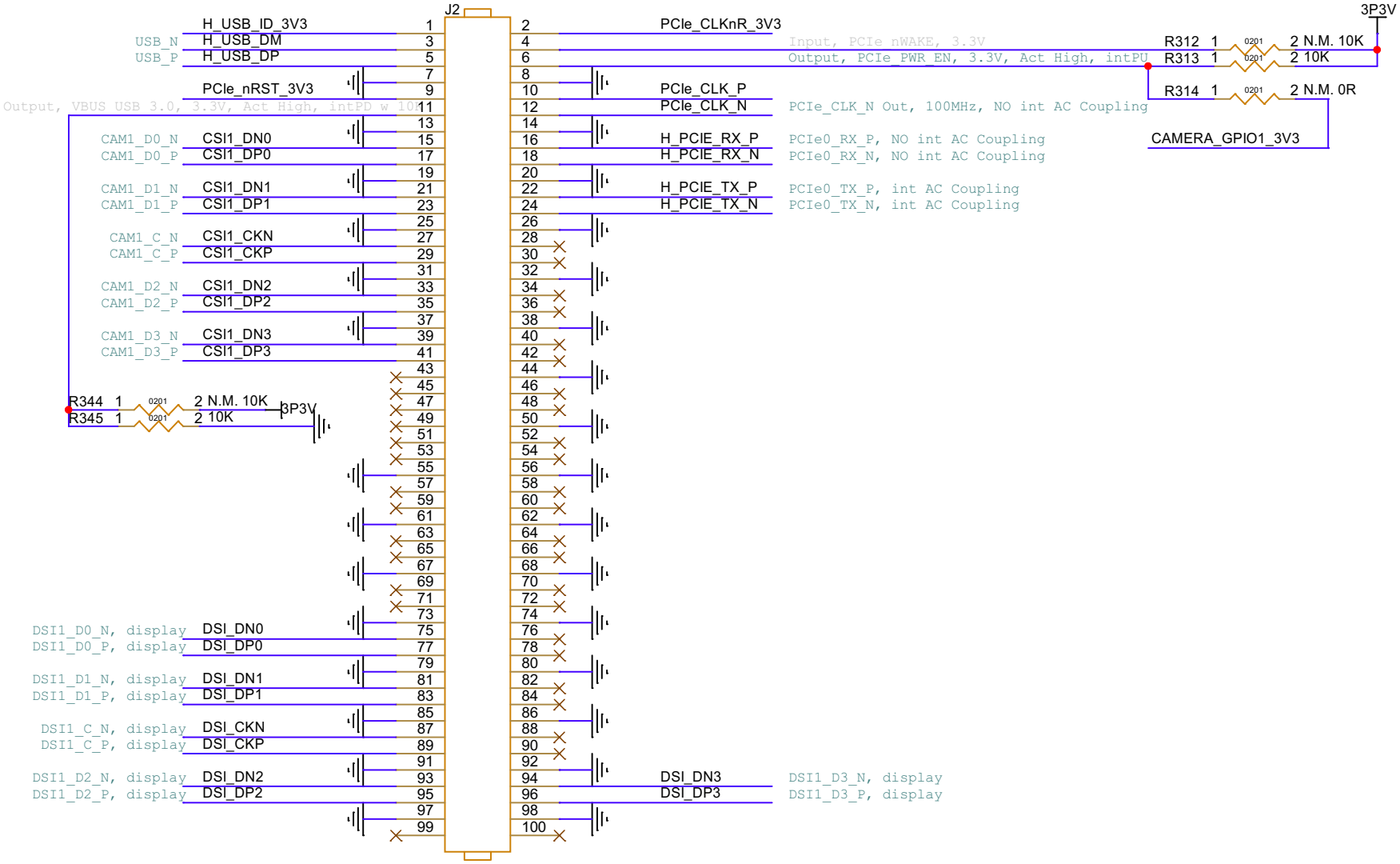
Pin number	Pin name	Pin description
40	GPIO_VREF_21	GPIO @ GPIO_VREF, intPU
41	GPIO_VREF_31	GPIO, UART2 RTS @ GPIO_VREF
42	GND	GND
43	GND	GND
44	GPIO_VREF_24	GPIO @ GPIO_VREF
45	GPIO_VREF_30	GPIO, UART2 CTS @ GPIO_VREF
46	GPIO_VREF_9	GPIO, UART2 TX @ GPIO_VREF
47	GPIO_VREF_8	GPIO, UART2 RX @ GPIO_VREF
48	GPIO_VREF_12	GPIO, UART3 RX @ GPIO_VREF
49	GPIO_VREF_18	GPIO @ GPIO_VREF
50	GPIO_VREF_11	GPIO, UART0 RTS @ GPIO_VREF
51	H_UART0_RXD_VREF	UART 0 RX @ GPIO_VREF
52	GND	GND
53	GND	GND
54	H_UART1_TXD_VREF	UART1 TX @ GPIO_VREF
55	H_UART0_TXD_VREF	UART0 TX @ GPIO_VREF
56	GPIO_VREF_6	GPIO, UART1 CTS, I2C2 SDA,...@ GPIO_VREF, intPU
57	SD_CLK	
58	GPIO_VREF_7	GPIO, UART1 RTS, I2C2 SCL,...@ GPIO_VREF, intPU
59	GND	GND

Pin number	Pin name	Pin description
60	GND	GND
61	SD_DATA3	SD_DAT3 @ 1.8V or 3.3V
62	SD_CMD	SD_CMD @ 1.8V or 3.3V
63	SD_DATA0	SD_DAT0 @ 1.8V or 3.3V
64	NC	
65	GND	GND
66	GND	GND
67	SD_DATA1	SD_DAT1 @ 1.8V or 3.3V
68	NC	
69	SD_DATA2	SD_DAT2 @ 1.8V or 3.3V
70	NC	
71	GND	GND
72	NC	
73	SD_VDD_OVERRIDE	Input, 3.3V, High if SD card 1.8V otherwise float, intPD w 1K
74	GND	GND
75	SD_PWR_ON_3V3	Output,3.3V, High to turn on SD card, intPU
76	NC	
77	5V_IN	5V PS IN (4.75V to 5.25V), 1.8A max (300mA per pin)
78	GPIO_VREF	GPIO_VREF, must be connected to 3.3V or 1.8V
79	5V_IN	5V PS IN (4.75V to 5.25V), 1.8A max (300mA per pin)

Pin number	Pin name	Pin description
80	H_I2C0_SCL_3V3	I2C0 SCL, 3.3V, Camera o Display, intPU 4.7V to 3.3V
81	5V_IN	5V PS IN (4.75V to 5.25V), 1.8A max (300mA per pin)
82	H_I2C0_SDA_3V3	I2C0 SDA, 3.3V, Camera o Display, intPU 4.7V to 3.3V
83	5V_IN	5V PS IN (4.75V to 5.25V), 1.8A max (300mA per pin)
84	3P3V	3.3V PS OUT, 600mA max (300mA per pin)
85	5V_IN	5V PS IN (4.75V to 5.25V), 1.8A max (300mA per pin)
86	3P3V	3.3V PS OUT, 600mA max (300mA per pin)
87	5V_IN	5V PS IN (4.75V to 5.25V), 1.8A max (300mA per pin)
88	1P8V	1.8V PS OUT, 600mA max (300mA per pin)
89	NC	
90	1P8V	1.8V PS OUT, 600mA max (300mA per pin)
91	NC	
92	RST_BUTTON	Input, 3.3V, Low to reset, intPU to 3.3V w 90K
93	BOOT_UART_N	Input, 3.3V, Low Boot from UART, intPU to 3.3V w 10K
94	USB_CC1	
95	PI_LED_nPWR	Out, 3.3V, Active Low, Power on LED, intPU
96	USB_CC2	
97	CAMERA_GPIO0_3V3	CAMERA_GPIO0, 3.3V
98	GND	GND
99	GLOBAL_EN	Input, 5V, Low to power off, intPU to 5V w 100K
100	H_RESETN_3V3 CAMERA_GPIO1_3V3	Output, 3.3V, Low during reset, intPU CAMERA_GPIO1, 3.3V, intPU

3.3.2 Carrier board connector (J2)

Figure 7 - Carrier board connector (J2)



Conn. 50x2 (Amphenol 10164228-1001A1RLF)

Table 2 - Carrier board connector 2 (J2) pinout

Pin number	Pin name	Pin description
1	H_USB_ID_3V3	
2	PCIe_CLKnR_3V3	Input, 3.3V, Active Low, intPD w 10K
3	H_USB_DM	USB_N
4		Input, PCIe_nWAKE, 3.3V
5	H_USB_DP	USB_P
6		Output, PCIe_PWR_EN, 3.3V, Active High, intPU
7	GND	GND
8	GND	GND
9	PCIe_nRST_3V3	PCIe, 3,3V, Active Low, intPU
10	PCIe_CLK_P	PCIe_CLK_P Out,100MHz, NO int AC Coupling
11		Output, VBUS USB 3.0, 3.3V, Active High, intPU,w 10K
12	PCIe_CLK_N	PCIe_CLK_N Out,100MHz, NO int AC Coupling
13	GND	GND
14	GND	GND
15	CSI1_DN0	CAM1_D0_N
16	H_PCIE_RX_P	PCIe0_RX_P, NO int AC Coupling
17	CSI1_DP0	CAM1_D0_P
18	H_PCIE_RX_N	PCIe0_RX_N, NO int AC Coupling
19	GND	GND
20	GND	GND

Pin number	Pin name	Pin description
21	CSI1_DN1	CAM1_D1_N
22	H_PCIE_TX_P	PCIe0_TX_P, int AC Coupling
23	CSI1_DP1	CAM1_D1_P
24	H_PCIE_TX_N	PCIe0_TX_N, int AC Coupling
25	GND	GND
26	GND	GND
27	CSI1_CKN	CAM1_C_N
28	NC	
29	CSI1_CKP	CAM1_C_P
30	NC	
31	GND	GND
32	GND	GND
33	CSI1_DN2	CAM1_D2_N
34	NC	
35	CSI1_DP2	CAM1_D2_P
36	NC	
37	GND	GND
38	GND	GND
39	CSI1_DN3	CAM1_D3_N
40	NC	

Pin number	Pin name	Pin description
41	CSI1_DP3	CAM1_D3_P
42	NC	
43	NC	
44	GND	GND
45	NC	
46	NC	
47	NC	
48	NC	
49	NC	
50	GND	GND
51	NC	
52	NC	
53	NC	
54	NC	
55	GND	GND
56	GND	GND
57	NC	
58	NC	
59	NC	
60	NC	

Pin number	Pin name	Pin description
61	GND	GND
62	GND	GND
63	NC	
64	NC	
65	NC	
66	NC	
67	GND	GND
68	GND	GND
69	NC	
70	NC	
71	NC	
72	NC	
73	GND	GND
74	GND	GND
75	DSI_DN0	DSI1_D0_N, display
76	NC	
77	DSI_DP0	DSI1_D0_P, display
78	NC	
79	GND	GND
80	GND	GND

Pin number	Pin name	Pin description
81	DSI_DN1	DSI1_D1_N, display
82	NC	
83	DSI_DP1	DSI1_D1_P, display
84	NC	
85	GND	GND
86	GND	GND
87	DSI_CKN	DSI1_C_N, display
88	NC	
89	DSI_CKP	DSI1_C_P, display
90	NC	
91	GND	GND
92	GND	GND
93	DSI_DN2	DSI1_D2_N, display
94	DSI_DN3	DSI1_D3_N, display
95	DSI_DP2	DSI1_D2_P, display
96	DSI_DP3	DSI1_D3_P, display
97	GND	GND
98	GND	GND
99	NC	
100	NC	

3.3.3 Carrier board connector (J4) (optional)

Figure 8 - Carrier board connector (J4)

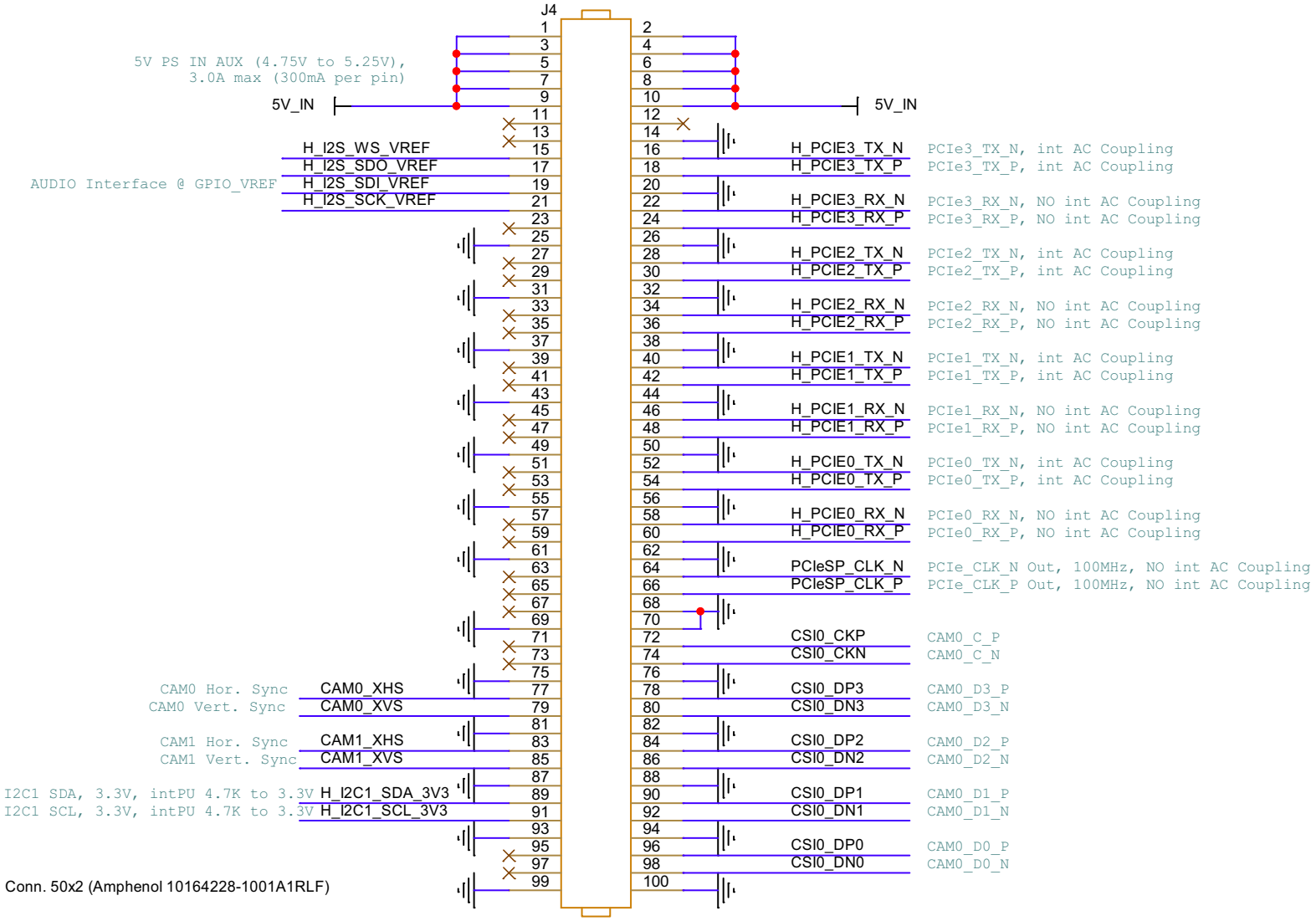


Table 3 - Carrier board connector 3 (J4)

Pin number	Pin name	Pin description
1	5V_IN	
2	5V_IN	
3	5V_IN	
4	5V_IN	
5	5V_IN	
6	5V_IN	
7	5V_IN	
8	5V_IN	
9	5V_IN	
10	5V_IN	
11	NC	
12	NC	
13	NC	
14	GND	GND
15	H_I2S_WS_VREF	
16	H_PCIE3_TX_N	PCIe3_TX_N, int AC Coupling
17	H_I2S_SDO_VREF	
18	H_PCIE3_TX_P	PCIe3_TX_P, int AC Coupling
19	H_I2S_SDI_VREF	AUDIO Interface @ GPIO_VREF
20	GND	GND

Pin number	Pin name	Pin description
21	H_I2S_SCK_VREF	
22	H_PCIE3_RX_N	PCIe3_RX_N, NO int AC Coupling
23	NC	
24	H_PCIE3_RX_P	PCIe3_RX_N, NOint AC Coupling
25	GND	GND
26	GND	GND
27	NC	
28	H_PCIE2_TX_N	PCIe2_TX_N, int AC Coupling
29	NC	
30	H_PCIE2_TX_P	PCIe2_TX_P, int AC Coupling
31	GND	GND
32	GND	GND
33	NC	
34	H_PCIE2_RX_N	PCIe2_RX_N, NO int AC Coupling
35	NC	
36	H_PCIE2_RX_P	PCIe2_RX_P, NO int AC Coupling
37	GND	GND
38	GND	GND
39	NC	
40	H_PCIE1_TX_N	PCIe1_TX_N, int AC Coupling

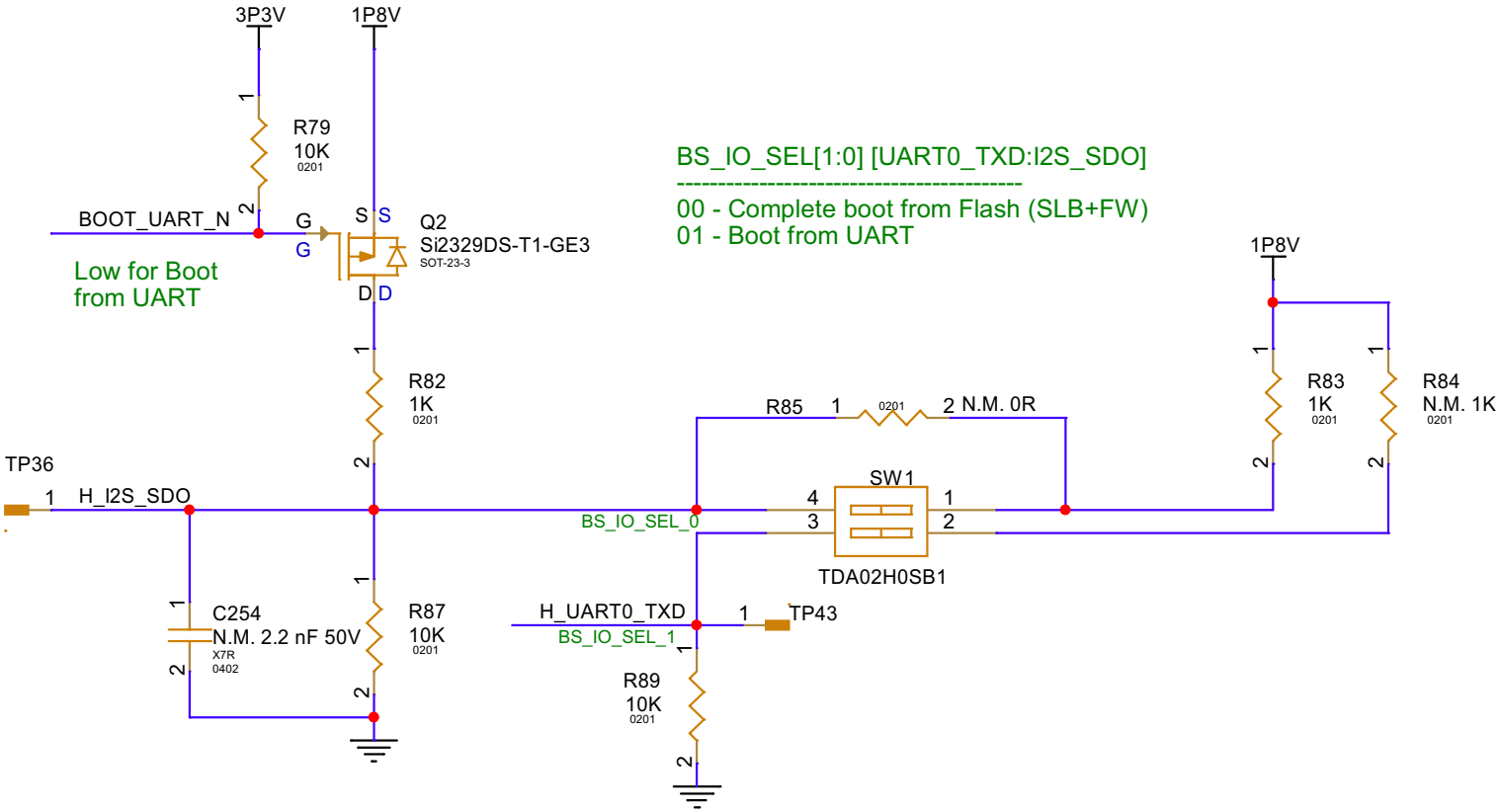
Pin number	Pin name	Pin description
41	NC	
42	H_PCIE1_TX_P	PCIe1_TX_P, int AC Coupling
43	GND	GND
44	GND	GND
45	NC	
46	H_PCIE1_RX_N	PCIe1_RX_N, NO int AC Coupling
47	NC	
48	H_PCIE1_RX_P	PCIe1_RX_P, NO int AC Couplin
49	GND	GND
50	GND	GND
51	NC	
52	H_PCIE0_TX_N	PCIe0_TX_N, int AC Coupling
53	NC	
54	H_PCIE0_TX_P	PCIe0_TX_P, int AC Coupling
55	GND	GND
56	GND	GND
57	NC	
58	H_PCIE0_RX_N	PCIe0_RX_N, NO int AC Coupling
59	NC	
60	H_PCIE0_RX_P	PCIe0_RX_P, NO int AC Coupling

Pin number	Pin name	Pin description
61	GND	GND
62	GND	GND
63	NC	
64	PCIeSP_CLK_N	PCIe_CLK_N Out, 100MHz, , NO int AC Coupling
65	NC	
66	PCIeSP_CLK_P	PCIe_CLK_P Out, 100MHz, , NO int AC Coupling
67	NC	
68	GND	GND
69	GND	GND
70	GND	GND
71	NC	
72	CSI0_CKP	CAM0_C_P
73	NC	
74	CSI0_CKN	CAM0_C_N
75	GND	GND
76	GND	GND
77	CAM0_XHS	CAM0 Horizontal Sync.
78	CSI0_DP3	CAM0_D3_P
79	CAM0_XVS	CAM0 Vertical Sync.
80	CSI0_DN3	CAM0_D3_N

Pin number	Pin name	Pin description
81	GND	GND
82	GND	GND
83	CAM1_XHS	CAM1 Horizontal Sync.
84	CSI0_DP2	CAM0_D2_P
85	CAM1_XVS	CAM1 Vertical Sync.
86	CSI0_DN2	CAM0_D2_N
87	GND	GND
88	GND	GND
89	H_I2C1_SDA_3V3	I2C1 SDA, 3.3V, intPU 4.7K to 3.3V
90	CSI0_DP1	CAM0_D1_P
91	H_I2C1_SCL_3V3	I2C1 SCL, 3.3V, intPU 4.7K to 3.3V
92	CSI0_DN1	CAM0_D1_N
93	GND	GND
94	GND	GND
95	NC	
96	CSI0_DP0	CAM0_D0_P
97	NC	
98	CSI0_DN0	CAM0_D0_N
99	GND	GND
100	GND	GND

3.4 Boot switch

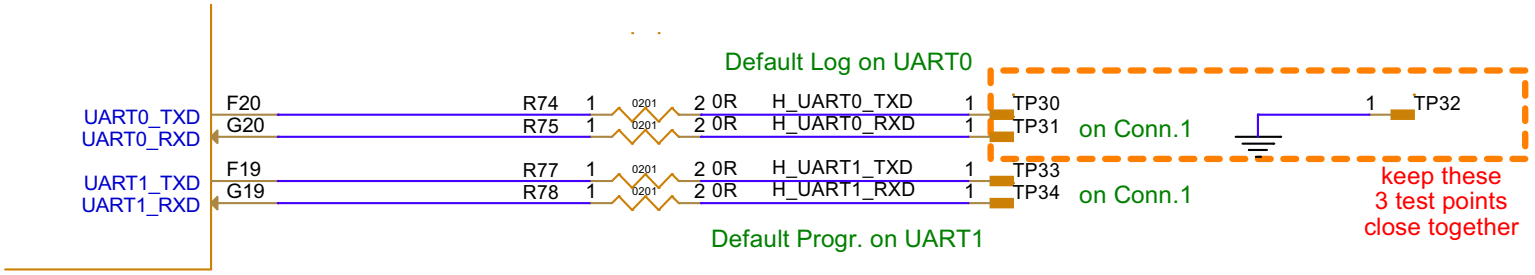
Figure 9 - Boot selection



Signal	Name and function	Description	Default
BS[O]	Debug ROM from RAM bs_arm_halt	If asserted, start with ARM halted upon power-up. In this mode, CORTEX PORESET is de-asserted while CORTEX SYSRESET Is kept asserted.	0
BS[1]	ROM source bs_boot_from_flash (load alternative ROM from flash)	If asserted, CORTEX is remapped to f lash in address 0 instead of ROM.	0
BS[2]	bs_bypass_fuse	Th is bootstrap will be available only with dedicated Debug package, and in product package, will not be exposed to avoid security breach.	0
BS[3:4]	bs_io_sel[1:0] i2s_sdo - bs_io_sel[0] uart0_tx - bs_io_se[1]	IO select decoding bs_io_sel[1:0] = 00 - Complete' boot from Flash (SLB+FW) (VPU + Accelerator) 01 - Boot from UART 10 - Boot from PCIe (Accelerator only) 11 - Secure debug flow selection (VPU + Accelerator)	00

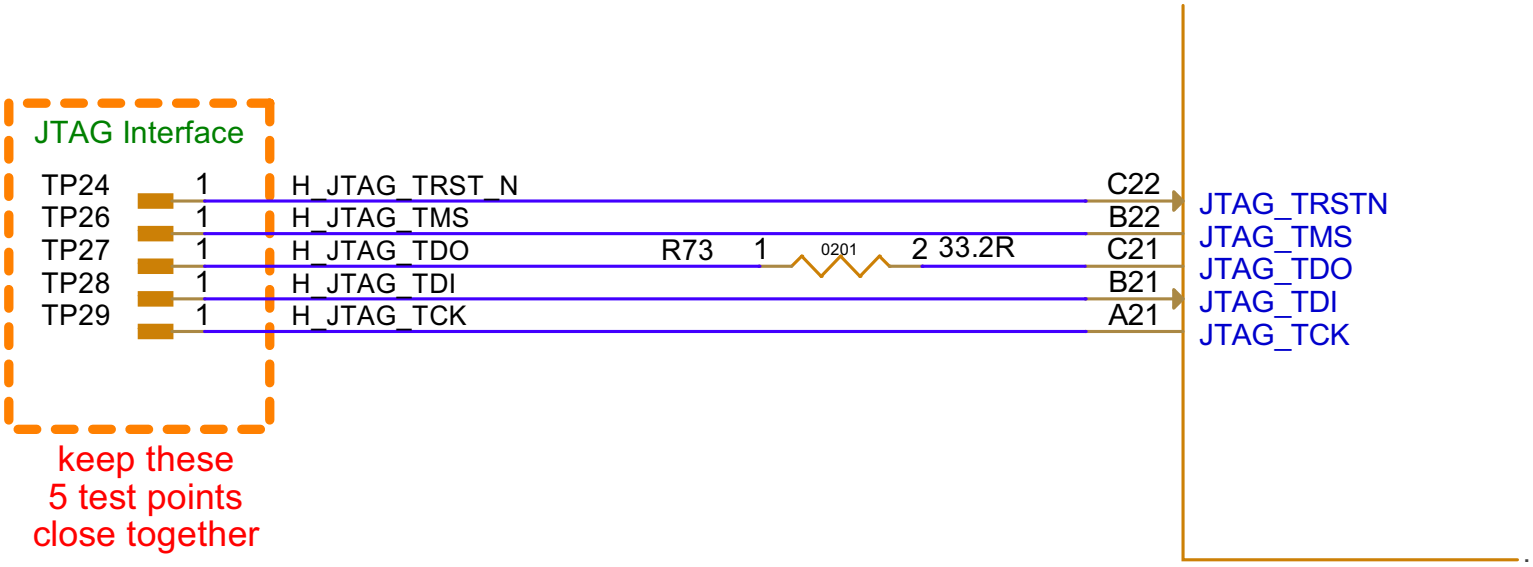
3.5 UART

Figure 10 - UART



3.6 JTAG

Figure 11 - JTAG interface



3.7 Pin configuration

				Alt. Func. - Valid Options (EACH GROUP OF PINS CAN ONLY BE SET TO THE SAME OPTION)										
GPIO H15	Func.	on Board	Default State	0 (default)	1	2	3	4	5	6	7	8	9
0	PI LED nACT (out, PU)	PU, isol	out, clk	init_debug0	X	GPIO0	i2c0 curr src en out	spi cs2	pwm0	safety out0	sdio0 gp out	UART2 TX	i2c2 curr src en out
1	GPIO + Alt. Func.	isol	out, clk	init_debug1	X	GPIO1	i2c1 curr src en out	spi cs3	pwm1	safety out0	sdio1 gp out	UART3 TX	i2c3 curr src en out
2	RST eMMC (out, INTERN, PU)	PU, isol	out,1	init_debug2	X	GPIO2	i2c0 curr src en out	isp spi trig out	pwm2	safety out0	usb vbus out	UART2 TX	i2c2 curr src en out
3	GPIO LED (out, INTERN, PD)	PD, isol	out,0	init_debug3	X	GPIO3	i2c1 curr src en out	isp pre spi out	pwm3	safety out1	sdio1 gp out	UART3 TX	i2c3 curr src en out
4	PI LED nPWR (out, PU)	PU, isol	out,0	init_debug4	X	GPIO4	GPIO4	GPIO4	pwm4	safety out0	sdio0 gp out	UART2 TX	i2c2 curr src en out
5	RST ETH (out, INTERN, PU)	PU, isol	out,1	init_debug5	X	GPIO5	i2c3 curr src en out	i2s sd1 in	pwm5	safety out1	sdio1 gp out	UART3 TX	usb vbus out
6	GPIO + Alt. Func.	PU	in,PD	UART1 CTS in	X	GPIO6	sdio0 wp in	parall data6	timer2 ext in	UART2 RX	I2C2 SDA	I2C3 SDA	UART3 CTS in
7	GPIO + Alt. Func.	PU	out,0	UART1 RTS out	X	GPIO7	sdio1 wp in	parall data7	timer3 ext in	UART3 RX	I2C2 SCL	I2C3 SCL	UART3 RTS out
8	GPIO + Alt. Func.		in,PD	GPIO8	X	GPIO8	GPIO8	parall data16	GPIO8	GPIO8	UART2 RX	X	X
9	GPIO + Alt. Func.		in,PD	sdio0 gp in	X	GPIO9	sdio0 gp in	parall data17	sdio0 gp in	sdio0 gp in	UART2 TX	X	X
10	GPIO + Alt. Func.	PU	in,PD	sdio0 cdin	X	GPIO10	sdio0 cd in	parall data18	sdio0 cd in	sdio0 cd in	UART0 CTS in	X	X
11	GPIO + Alt. Func.		in,PD	usb ovrc in	X	GPIO11	usb ovrc in	parall data19	GPIO11	usb ovrc in	UART0 RTS out	X	X
12	GPIO + Alt. Func.		out,0	usb vbus out	X	GPIO12	usb vbus out	parall data20	safety out1	usb vbus out	UART3 RX	X	X
13	GPIO + Alt. Func.		in,PD	sdio1 gp in	X	GPIO13	i2c1 curr src en out	parall data21	GPIO13	sdio1 gp in	UART3 TX	X	X
14	GPIO + Alt. Func.	PU	in,PD	sdio1 cd in	X	GPIO14	GPIO14	parall data22	safety out0	sdio0 cd in	GPIO14	X	X
15	PCIe RESN (out, PU)	PU	out,0	mpp res out	X	GPIO15	mpp res out	parall data23	mpp res out	GPIO15	mpp res out	X	X
16	SD PW ON (out, PU)	PU	in,PD	GPIO16	X	GPIO16	GPIO16	parall data8	UART2 RX	GPIO16	X	X	X
17	CAMERA GPIO0 (IO)		in,PD	GPIO17	X	GPIO17	GPIO17	parall data9	UART2 TX	GPIO17	X	X	X
18	GPIO + Alt. Func.		in,PD	timer0 ext in	X	GPIO18	timer0 ext in	parall data10	timer0 ext in	timer0 ext in	X	X	X
19	GPIO + Alt. Func.		in,PD	timer1 ext in	X	GPIO19	timer1 ext in	parall data11	timer1 ext in	timer1 ext in	X	X	X
20	GPIO + Alt. Func.	PU	in,PD	GPIO20	X	GPIO20	GPIO20	parall data12	I2C3 SDA	GPIO20	pwm0	X	X
21	GPIO + Alt. Func.	PU	in,PD	GPIO21	X	GPIO21	GPIO21	parall data13	I2C3 SCL	GPIO21	pwm1	X	X
22	GPIO + Alt. Func.	PU	in,PD	GPIO22	X	GPIO22	I2C2 SDA	parall data14	I2C2 SDA	GPIO22	X	X	X
23	GPIO + Alt. Func.	PU	in,PD	GPIO23	X	GPIO23	I2C2 SCL	parall data15	I2C2 SCL	GPIO23	X	X	X
24	GPIO + Alt. Func.		in,PD	i2s sd1 in	X	GPIO24	i2c2 curr src en out	parall hsync	i2c0 curr src en out	GPIO24	X	X	X
25	GPIO + Alt. Func.		out,0	i2c0 curr src en out	X	GPIO25	i2c0 curr src en out	parall vsync	i2c1 curr src en out	i2c0 curr src en out	X	X	X
26	GPIO + Alt. Func.		out,0	i2c1 curr src en out	X	GPIO26	i2c1 curr src en out	parall data0	UART1 CTS in	i2c1 curr src en out	sdio1 gp in	X	X
27	GPIO + Alt. Func.		out,0	pwm0	X	GPIO27	GPIO27	parall data1	UART1 RTS out	GPIO27	cpu trace clk	X	X
28	ENET SYNC OUT (out)		out,0	pwm1	X	GPIO28	GPIO28	parall data2	UART2 CTS in	GPIO28	cpu trace d0	X	X
29	CAMERA GPIO1 (IO, PU)	PU	in,PD	GPIO29	X	GPIO29	GPIO29	parall data3	UART2 RTS out	GPIO29	cpu trace d1	X	X
30	GPIO + Alt. Func.		in,PD	UART0 CTS in	X	GPIO30	UART0 CTS in	parall data4	UART2 CTS in	GPIO30	cpu trace d2	X	X
31	GPIO + Alt. Func.		out,0	UART0 RTS out	X	GPIO31	UART0 RTS out	parall data5	UART2 RTS out	GPIO31	cpu trace d3	X	X

... Incorrect/incompatible pin configuration

... Other specific pins, compatible, but not essential

... GPIO

... UART1 CTS/RTS

... Sdio 0/1 Card detect (not used)

... MPP Reset (PCIe reset)

... PWM 0/1

... UART0 CTS/RTS

... I2C2

... I2C3

... UART2 TX/RX/CTS/RTS

... UART2 CTS/RTS dual (in the same configuration of the bench that is already there)

4 Maintenance and disposal

4.1 Routine maintenance

Check the Astrial H15 module and clean the contacts and printed circuit boards, paying particular attention to their condition.

Remove dust using dry air jets.

Do not use water, petrol or other flammable solvents, always use non-toxic commercial solvents.

Do not use dirty, stringy or abrasive rags.

WARNING

Dust hazard!

Dust can pose a danger because it can be rich in electrostatic charges which can interfere, even severely, with operation of the circuit.

Oxidation phenomena can occur on the arts of the circuit board that fit into the various slots of the equipment. To keep the equipment in good working order at all times, clean the printed circuit boards periodically.

Caution

Risk of damage!

Take care not to damage the printed circuit boards and/or connector contacts.

4.2 Decommissioning and disposal

WARNING

Risk of electric shock!

Switch off the power supply before disconnecting the cables and dismantle the parts to be disposed of.

The Astrial H15 module must be dismantled and disassembled completely before being disposed of.

- Plastic enclosure parts must be taken to a plastic recycling centre.
- Stainless steel parts must be taken to a metal recycling centre.
- Electronic components and/or printed circuit boards must be disposed of in compliance with national regulations for the disposal of electronic products.

WARNING

Dispose of materials safely!

Dispose of the various materials so that they can be recycled in compliance with the regulations in force in the country of use.

Nationally, the European Union Act 2018 amended Legislative Decree 49/2014, in compliance with Directive 2012/19/EU on waste electrical and electronic equipment (WEEE).

5 Technical support

In case of any queries, please contact System Electronics.

Always specify:

- The customer name and identification data.
- The product identification data, such as code and model.

Contact information:

System Electronics

Via Ghiarola Vecchia, 73

41042 Fiorano (MO) - Italy

www.systemelectronics.com

e-mail: info@systemelectronics.com

Systemelectronics.ai

Information

Always purchase original or equivalent spare parts if authorised in writing by System Electronics.

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